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DUO-MODE KEEPER CIRCUIT

CROSS REFERENCE TO RELATED APPLICATION

The present invention is related to the following: U.S. Patent Application Serial No. 10/155,375 (Attorney Docket No. AUS920030497US1), filed concurrently with this application, entitled "LIMITED SWITCH DYNAMIC LOGIC CIRCUIT WITH KEEPER," and

U.S. Patent Application Serial No. 10/116,612, filed April 4, 2002, entitled "CIRCUITS AND SYSTEMS FOR LIMITED SWITCH DYNAMIC LOGIC," which are incorporated by reference herein.

TECHNICAL FIELD

The present invention relates in general to metal oxide silicon (MOS) dynamic logic circuits.

BACKGROUND INFORMATION

Modern data processing systems may perform Boolean operations on a set of signals using dynamic logic circuits. Dynamic logic circuits are clocked. During the precharge phase of the clock, the circuit is preconditioned, typically by precharging an internal node (dynamic node) of the circuit by coupling to a power supply rail. During an evaluate phase of the clock, the Boolean function being implemented by the logic circuit is evaluated in response to the set of input signal values appearing on the inputs during the evaluate phase. (For the purposes herein, it suffices to assume that the input signals have settled to their "steady-state" values for the current clock cycle, recognizing that the input value may change from clock cycle to clock cycle.) Such dynamic logic may have advantages in both speed and the area consumed on the chip over static logic. However, the switching of the output node with the toggling of the phase of the clock each cycle may consume power even when the logical value of the output is otherwise unchanged.